Design and Verification of an Application Specific Integrated Circuit (ASIC)

Senior Project II



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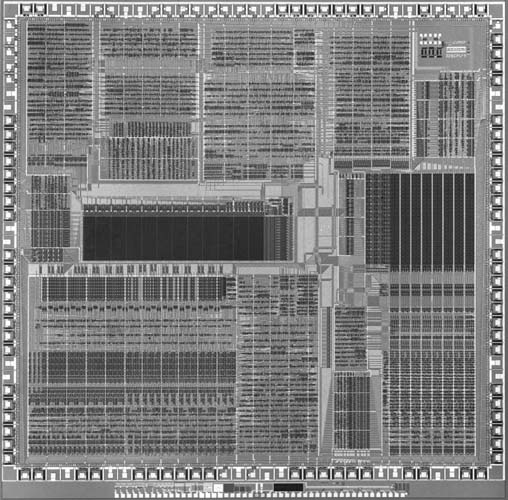
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**Fulfillment Page**



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**Acknowledgements**

**Zach**

**Abstract**

The goal of this project is to gain experience in VLSI design by designing a chip that will process digital streaming audio data. More specifically, we will implement a 512-tap digital finite impulse response (FIR) filter, which will be applied to an input stream in order to create an output stream. We used the I2C protocol to allow a host to control the chip and the serial I2S protocol for transferring digital audio streams in and out.

Our hardware design was represented using Verilog register-transfer level (RTL) code. Development has been done using Xilinx ISE Design Suite 14.7. Test-benches were also designed and implemented using Verilog. The end goal of the project is to implement the design on a field-programmable gate array (FPGA). We will bring up our FPGA design with a realistic environment including an audio source, audio sink, and a microcontroller for reading and writing registers. We also plan to send a simple CMOS integrated circuit design for fabrication by MOSIS that will help us gain experience in physical chip design and prepare future groups to fabricate our full design.

**Keywords:** Application-specific integrated circuit (ASIC), Very large scale integration (VLSI) I2S, I2C, Digital filtering

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**Nomenclature**

**ASIC**: Application Specific Integrated Chip

**BIST**: Built in Self-Test

**CIF**: Caltech Intermediate Form

**DIP**: Dual in-line package

**EDA**: Electronic Design Automation

**FPGA**: Field Programmable Gate Architecture

**FSM**: Finite-State Machine

**GDSII**: Graphic Data System II

**I2C**: Inter-Integrated Circuit

**I2S**: Integrated Interchip Sound

**IC**: Integrated Circuit

**LSB**: Least Significant Bit

**MEP**: MOSIS Educational Program

**MPW**: Multi-Project Wafer

**MSB**: Most Significant Bit

**OCP**: Open Cavity Plastic

**PCB**: Printed Circuit Board

**RO**: Read Only

**RTL**: Register-Transfer Level

**RTR**: Ready to Receive

**RTS**: Ready to Send

**RW**: Read/Write

**WO**: Write Only

**XFC**: Transfer Complete

**VLSI:** Very Large Scale Integration

**Introduction**

Zach

**Specifications**

**General:**

**I2S:**

**Filter:**

**I2C:**

**Register:**

**Chapter 1: Background – Z. Nelson**

**Chapter 2: System Design – Z. Nelson**

**Chapter 3: I2S Interface – K. Cao**

**Chapter 4: Digital Filtering – D. Naik**

**Chapter 5: Register Block – J. Swift**

**Chapter 6: I2C Slave Interface – W. Forman**

**Chapter 7: Simulation/Verficiation – K. Cao and W. Forman**

**Chapter 8: FPGA Implementation - Zachary Nelson**

**Chapter 9: EDA Tools and Physical Design – D. Naik**

**and J. Swift**

**Chapter 10: Conclusion**

**References**

[1] Mosis.com, ‘About Us’, 2015.[Online]. Available: https://www.mosis.com/what-is-mosis. [Accessed: 11 November 2015].

[2] nxp.com, ‘*I2C-bus specification and user manual - UM10204*’, 2015. [Online]. Available: <http://www.nxp.com/documents/user_manual/UM10204.pdf>. [Accessed: 10 November 2015]

**Appendix A: Project Overview**

**Biography:**

* Kevin Cao
  + Kevin is from Morris Plains, NJ and is a Computer Engineering major who is planning to enter the workforce after graduating at TCNJ. Kevin has interned as a software engineer at LGS Innovations, located in Florham Park, NJ.
* Whitley Forman
  + Whitley is from Ocean Grove, NJ and is an Electrical Engineering major who is continuing his education in the electrical field and will be obtaining his Master Electrician’s license after graduation. He is planning on using his new knowledge and experience with his current business to expand into new ventures.
* Dhruvit Naik
  + A resident of Mount Laurel, NJ, Dhruvit is a senior Computer Engineering major at TCNJ. He plans on entering the workforce after graduation and continuing his education in the coming years. He is the Vice-President of a startup, ThinkSOAS, INC.
* Zachary Nelson
  + From Cream Ridge, NJ, Zachary is a Computer Engineering major who is planning on attending graduate school after graduation. He has experience as a software engineering intern at Teletronics Technology Corporation and an undergraduate student researcher at TCNJ as part of the MUSE program.

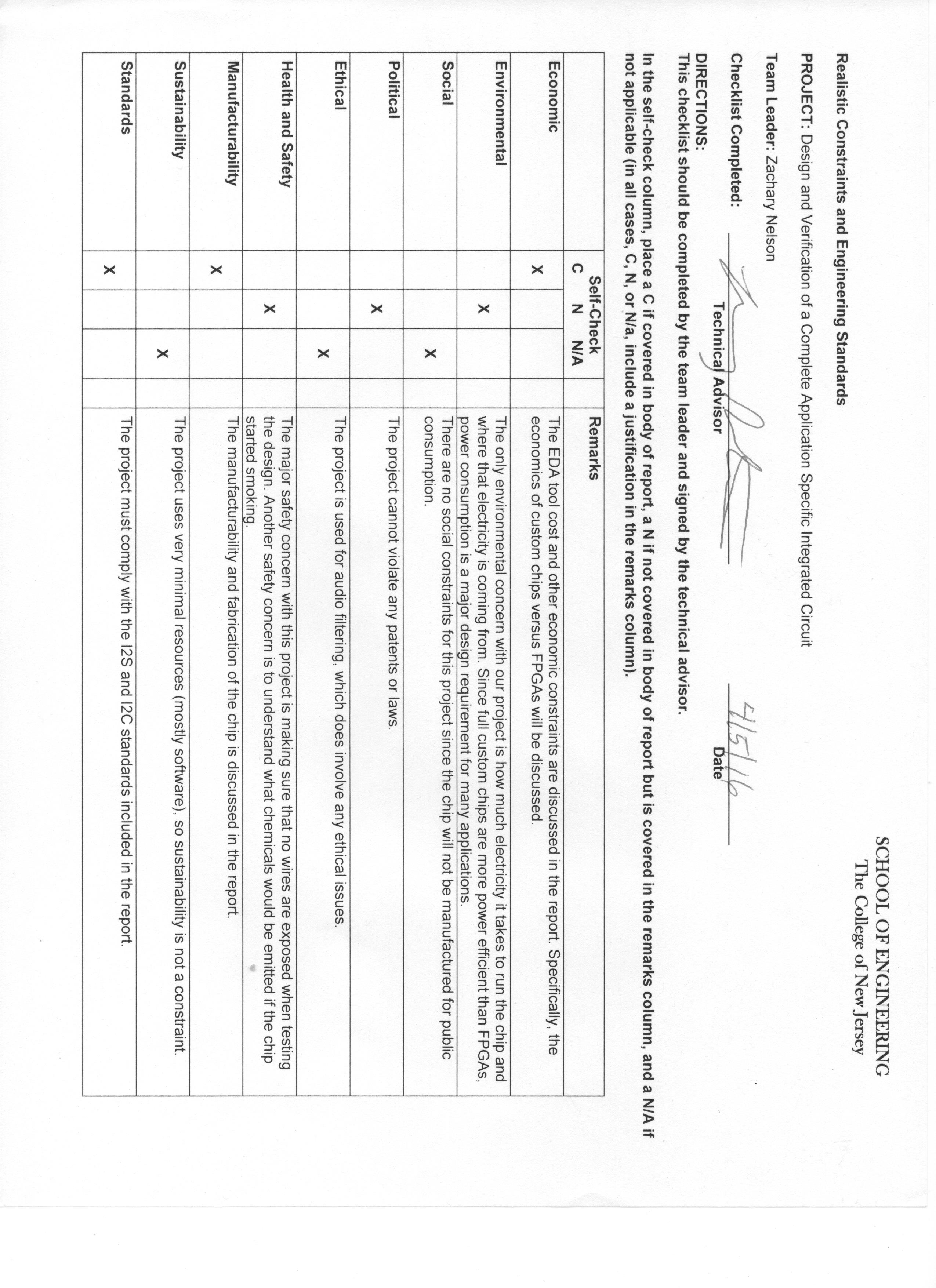


* Julie Swift



From Robbinsville, NJ Juliann is a Computer Engineering major who is planning on entering the workforce after college. She has experience as a AutoCAD Designer interning at Linearization Technology and a Software Development Life Cycle Analyst interning at Educational Testing Services. She participated in the undergraduate student research program, MUSE, at TCNJ.

**Engineering Standards and Realstic Contraints Form:**



**Engineering Standards, Specfications, and Codes:**

**Modern Engineering Tools:**

**Appendix B: Management**

**Schedule:**

**Meeting Minutes:**

**List of Contacts:**

**Material List:**

**Financial Budget:**

|  |  |  |
| --- | --- | --- |
| **Item** | **Cost** | **Comment** |
| ISE Design Suite 14.7 | $0.00 | Free software |
| CORE 9 University | $0.00 | Vitech’s CORE in the Classroom program |
| Dropbox | $0.00 | Free up to 2GB of storage |
| Git/GitHub Desktop | $0.00 | Free software |
| Microsoft Project 2013 | $0.00 | Free from the Computer Science Department’s DreamSpark Program |
| Mentor Graphics | $0.00 | TCNJ Subscription |
| Linux RedHat Operating System | $0.00 | TCNJ Subscription |
| Nexys 4 Artix-7 FPGA Board | $192.41 | Purchased from Digilent |
| UDA 1380 Board | $20.00 | Needs to be purchased |
| Crystal Oscillators | $20.00 | Needs to be purchased |
| CY8CKIT-050 PSoC 5LP Development Kit | $0.00 | School already owns |
| **Total Budget** | $500.00 |  |
| **Total Costs** | $232.41 |  |
| **End Balance** | $267.59 | Well under-budget |

**Appendix C: Source Code**

**Appendix D: Test Benches**

**Appendix E: Industry Specficiations**