Design and Verification of an Application Specific Integrated Circuit (ASIC)

Senior Project II



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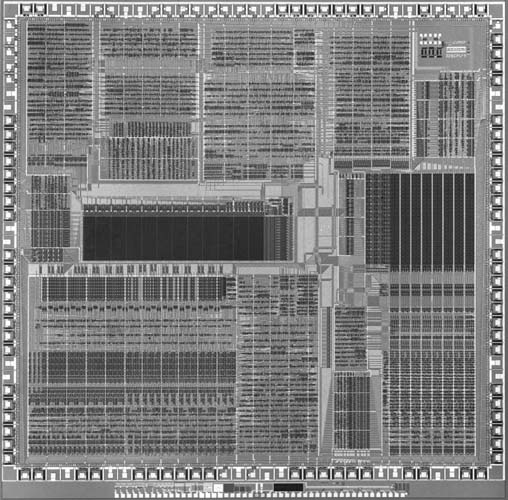
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**Fulfillment Page**



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**Abstract**

**Keywords:**

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**Acronyms**

**ASIC**: Application Specific Integrated Chip

**BIST**: Built in Self-Test

**CIF**: Caltech Intermediate Form

**DIP**: Dual in-line package

**EDA**: Electronic Design Automation

**FPGA**: Field Programmable Gate Architecture

**FSM**: Finite-State Machine

**GDSII**: Graphic Data System II

**I2C**: Inter-Integrated Circuit

**I2S**: Integrated Interchip Sound

**IC**: Integrated Circuit

**LSB**: Least Significant Bit

**MEP**: MOSIS Educational Program

**MPW**: Multi-Project Wafer

**MSB**: Most Significant Bit

**OCP**: Open Cavity Plastic

**PCB**: Printed Circuit Board

**RO**: Read Only

**RTL**: Register-Transfer Level

**RTR**: Ready to Receive

**RTS**: Ready to Send

**RW**: Read/Write

**WO**: Write Only

**XFC**: Transfer Complete

**VLSI:** Very Large Scale Integration

**Introduction**

**Specifications**

**General:**

**I2S:**

**Filter:**

**I2C:**

**Register:**

**Chapter 1: Background - Zachary Nelson**

**Chapter 2: I2S Interface - Kevin Cao**

**Chapter 3: Digital Filtering - Dhruvit Naik**

**Chapter 4: Register Block - Julie Swift**

**Chapter 5: I2C Slave Interface - Whitley Forman**

**Chapter 6: Budget - Zachary Nelson**

**Chapter 7: Schedule - Zachary Nelson**

**Chapter 8: Conclusion**

**References**

[1] Mosis.com, ‘About Us’, 2015.[Online]. Available: https://www.mosis.com/what-is-mosis. [Accessed: 11 November 2015].

[2] nxp.com, ‘*I2C-bus specification and user manual - UM10204*’, 2015. [Online]. Available: <http://www.nxp.com/documents/user_manual/UM10204.pdf>. [Accessed: 10 November 2015]

**Appendix A: Biography**

* Kevin Cao
  + Kevin is from Morris Plains, NJ and is a Computer Engineering major who is planning to enter the workforce after graduating at TCNJ. Kevin has interned as a software engineer at LGS Innovations, located in Florham Park, NJ.
* Whitley Forman
  + Whitley is from Ocean Grove, NJ and is an Electrical Engineering major who is continuing his education in the electrical field and will be obtaining his Master Electrician’s license after graduation. He is planning on using his new knowledge and experience with his current business to expand into new ventures.
* Dhruvit Naik
  + A resident of Mount Laurel, NJ, Dhruvit is a senior Computer Engineering major at TCNJ. He plans on entering the workforce after graduation and continuing his education in the coming years. He is the Vice-President of a startup, ThinkSOAS, INC.
* Zachary Nelson
  + From Cream Ridge, NJ, Zachary is a Computer Engineering major who is planning on attending graduate school after graduation. He has experience as a software engineering intern at Teletronics Technology Corporation and an undergraduate student researcher at TCNJ as part of the MUSE program.4



* Julie Swift



From Robbinsville, NJ Juliann is a Computer Engineering major who is planning on entering the workforce after college. She has experience as a AutoCAD Designer interning at Linearization Technology and a Software Development Life Cycle Analyst interning at Educational Testing Services. She participated in the undergraduate student research program, MUSE, at TCNJ.

**Appendix B: Gantt Chart**

**Appendix C: Financial Budget**

|  |  |  |
| --- | --- | --- |
| **Item** | **Cost** | **Comment** |
| ISE Design Suite 14.7 | $0.00 | Free software |
| CORE 9 University | $0.00 | Vitech’s CORE in the Classroom program |
| Dropbox | $0.00 | Free up to 2GB of storage |
| Git/GitHub Desktop | $0.00 | Free software |
| Microsoft Project 2013 | $0.00 | Free from the Computer Science Department’s DreamSpark Program |
| Mentor Graphics | $0.00 | TCNJ Subscription |
| Linux RedHat Operating System | $0.00 | TCNJ Subscription |
| Nexys 4 Artix-7 FPGA Board | $192.41 | Purchased from Digilent |
| UDA 1380 Board | $20.00 | Needs to be purchased |
| Crystal Oscillators | $20.00 | Needs to be purchased |
| CY8CKIT-050 PSoC 5LP Development Kit | $0.00 | School already owns |
| **Total Budget** | $500.00 |  |
| **Total Costs** | $232.41 |  |
| **End Balance** | $267.59 | Well under-budget |

**Appendix D: Engineering Standards and Realistic Constrainsts Form**

**Appendix E: Realistic Constraints in Design Project**

**Appendix F1: Engineering Standards in Design Project**

**Appendix F2: Three Laws of Marekting**

**Appendix F3: Milestone Resultant Evulation**

**Appendix G: Verilog Code**

**Appendix F: Verilog Test Benchs**